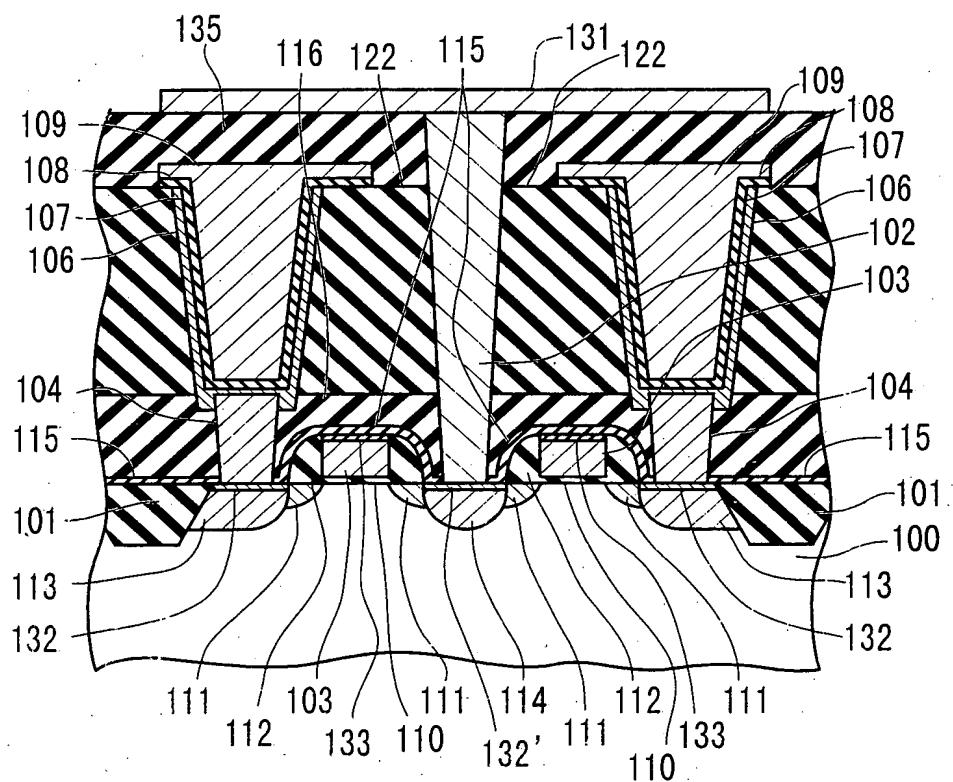


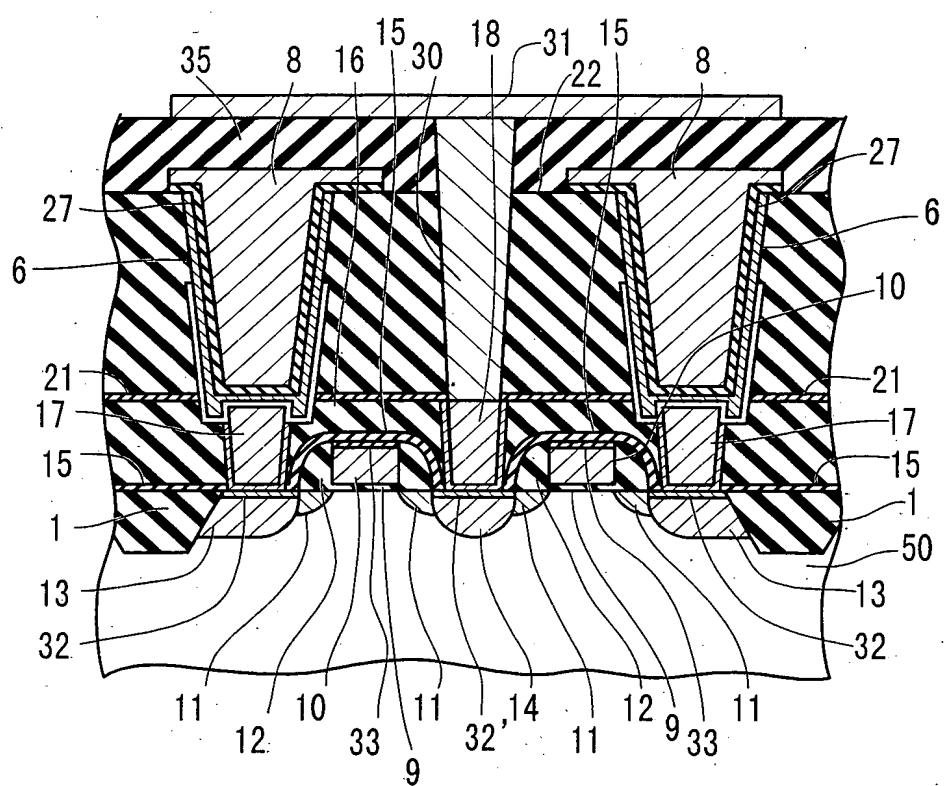


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Fig. 1 PRIOR ART



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Fig. 3

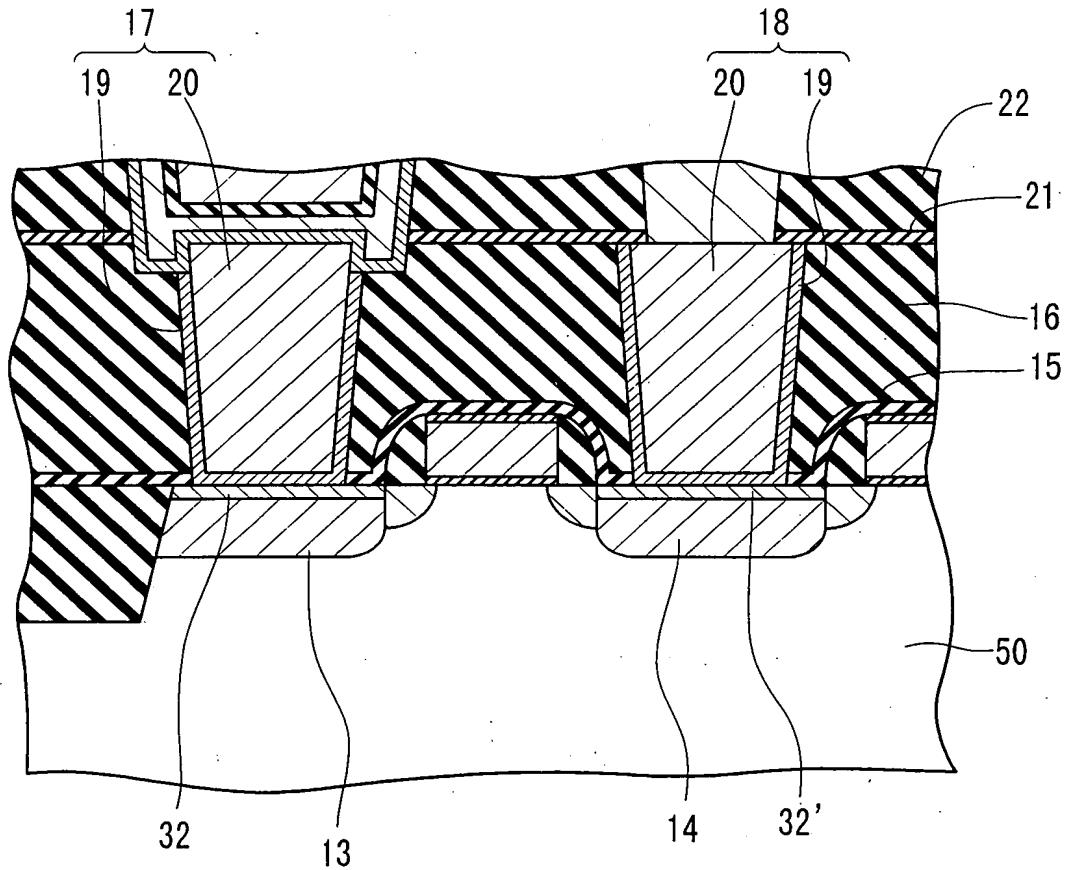




Fig. 4

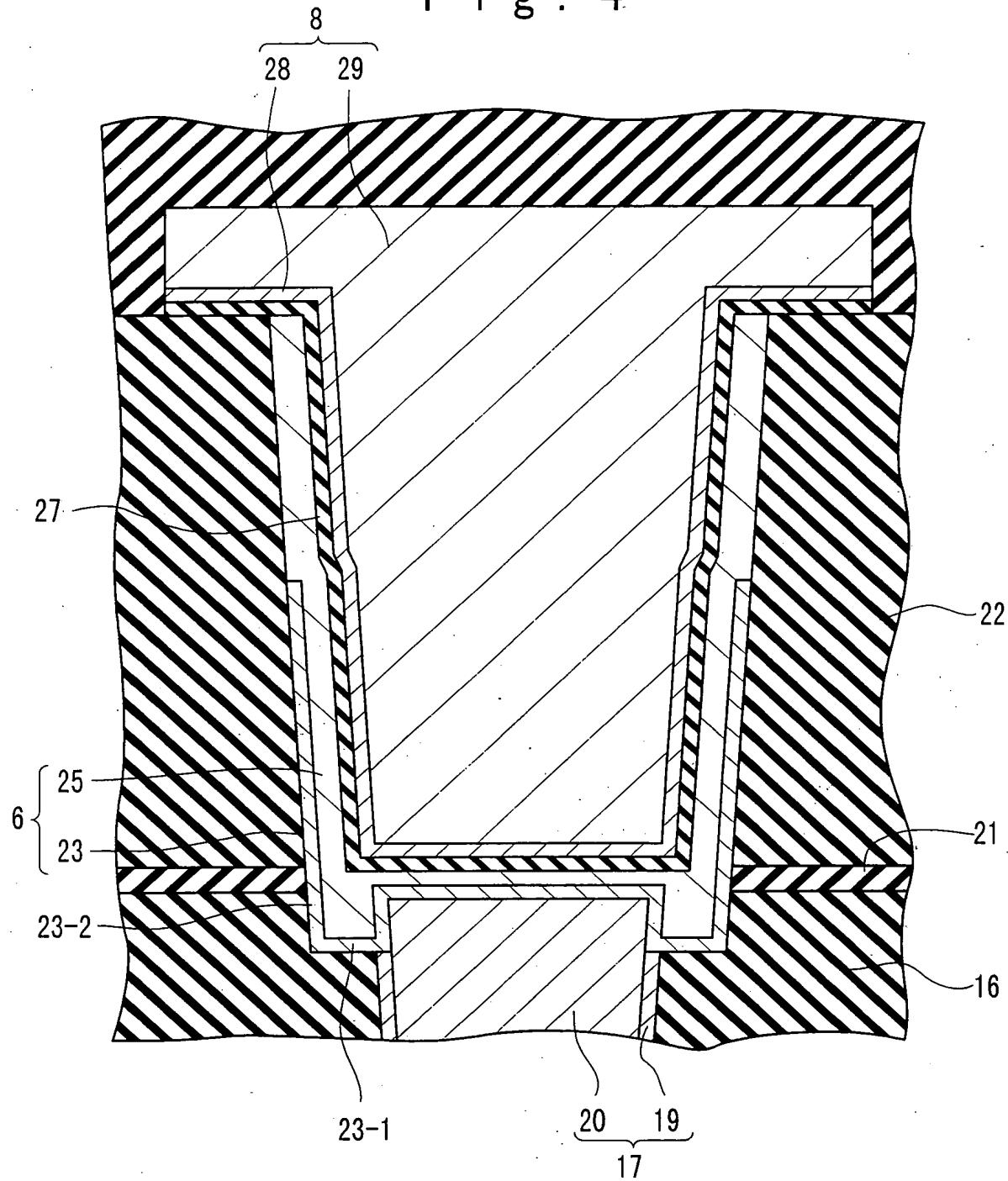
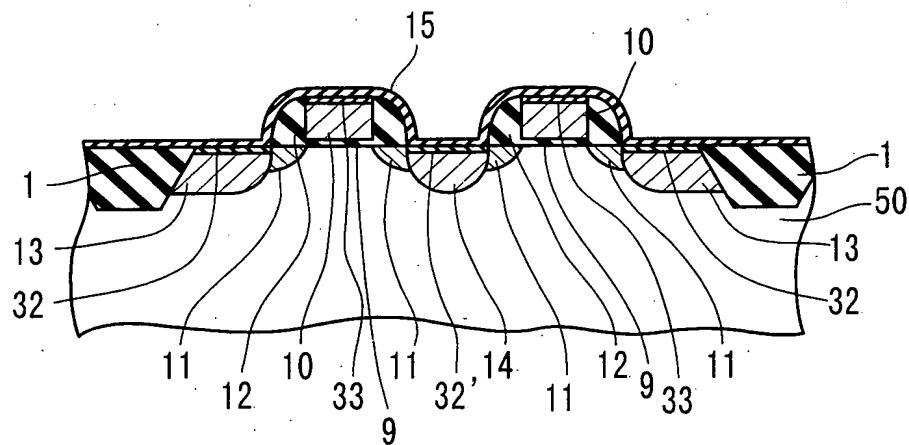




Fig. 5



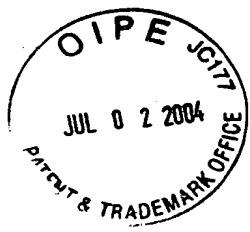


Fig. 6

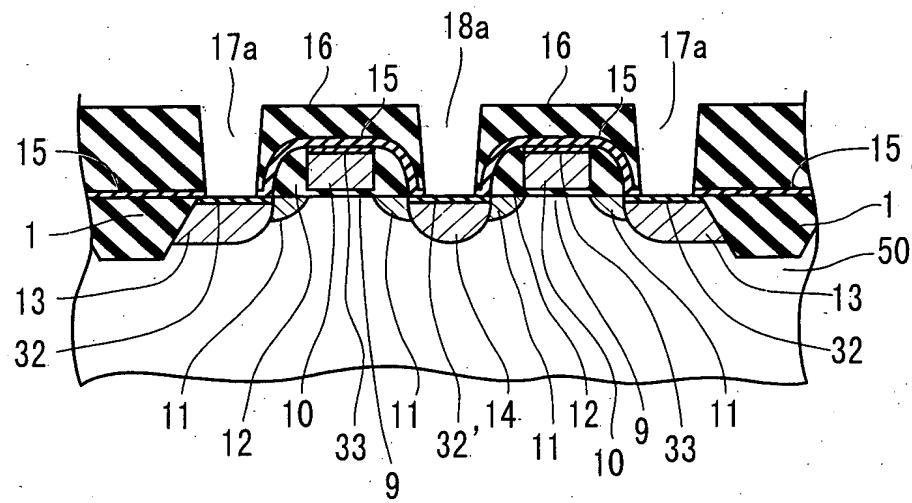
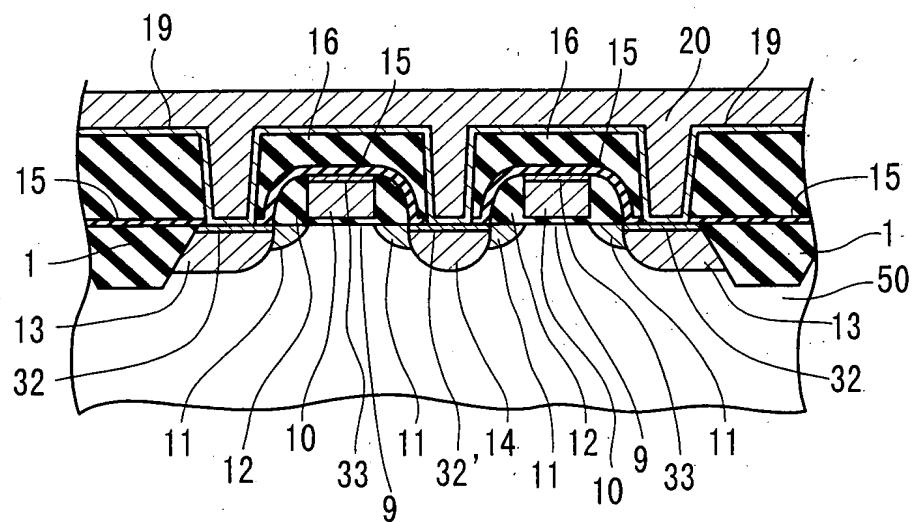


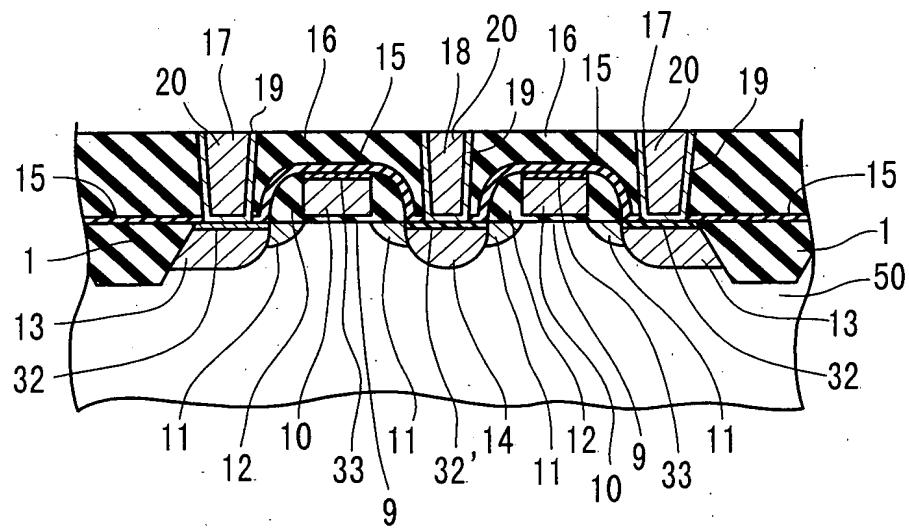


Fig. 7



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Fig. 9

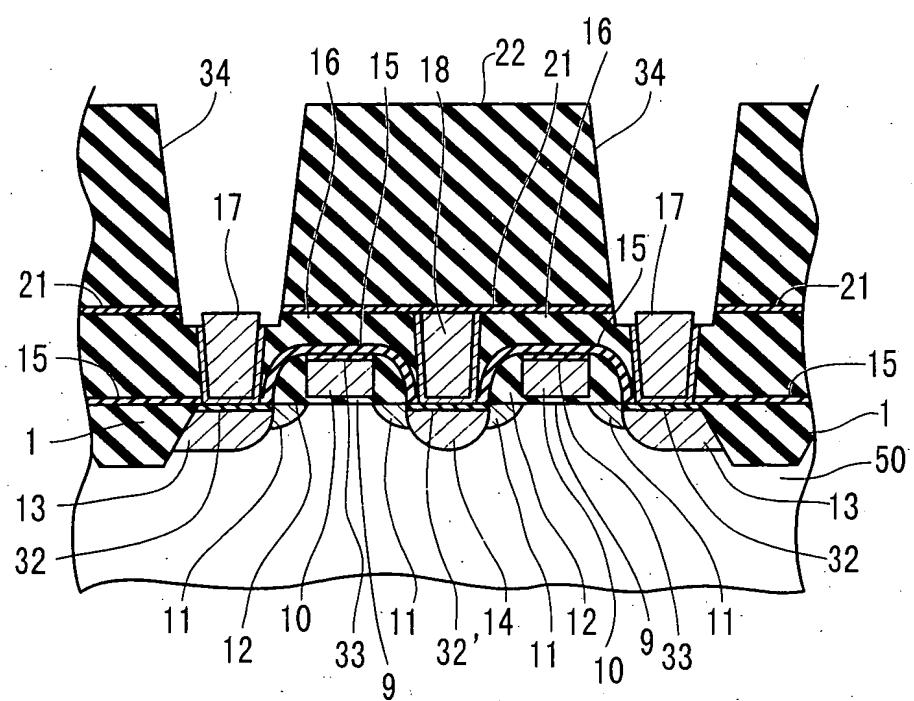
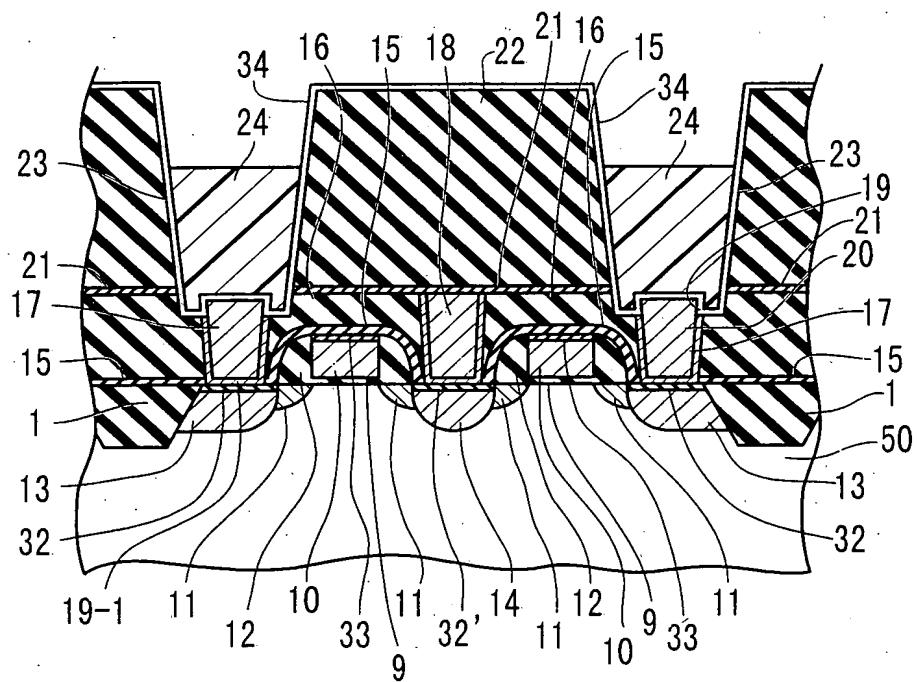


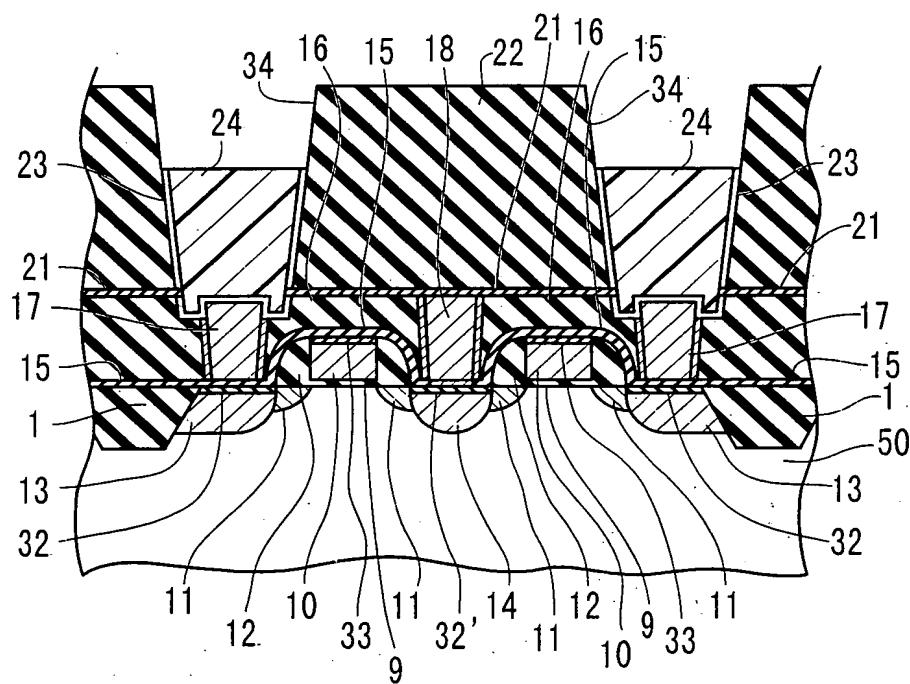
Fig. 10



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Fig. 11





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Fig. 12

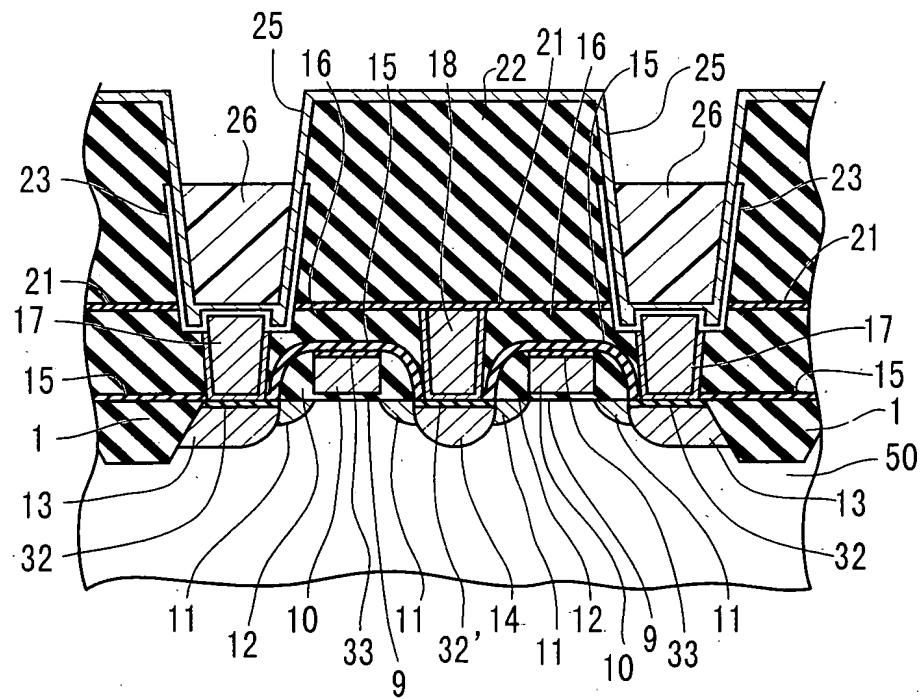
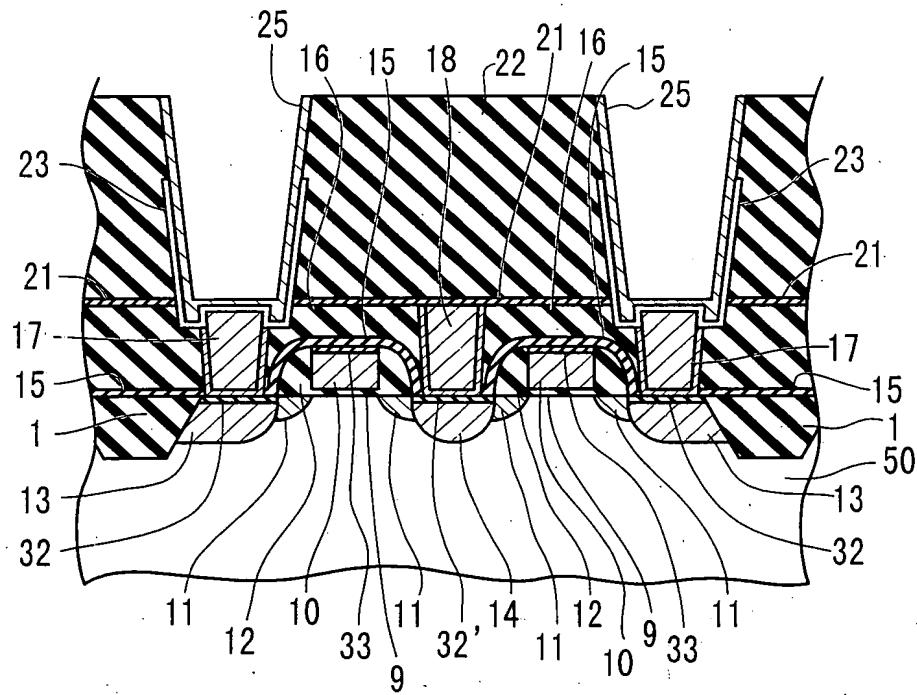


Fig. 13





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Fig. 14

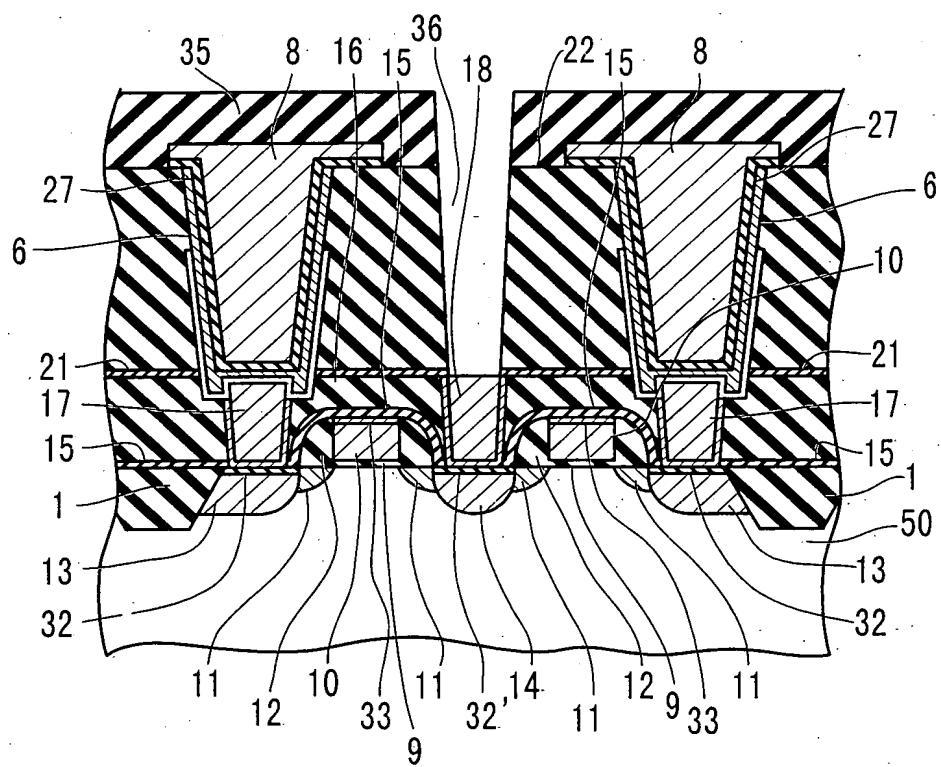


Fig. 15

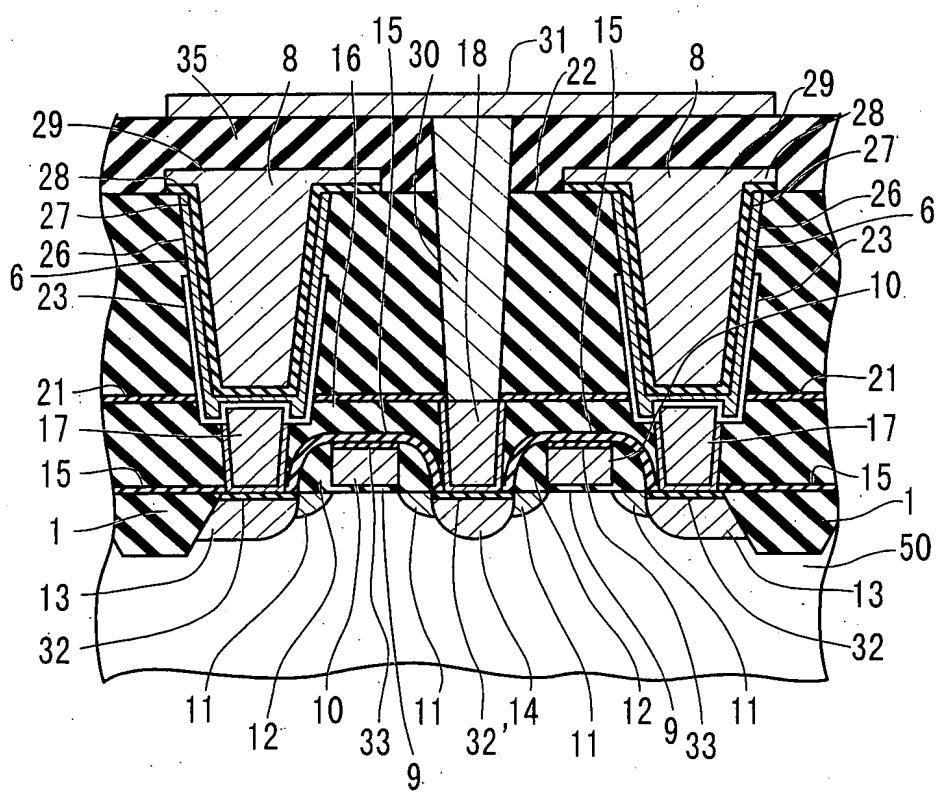
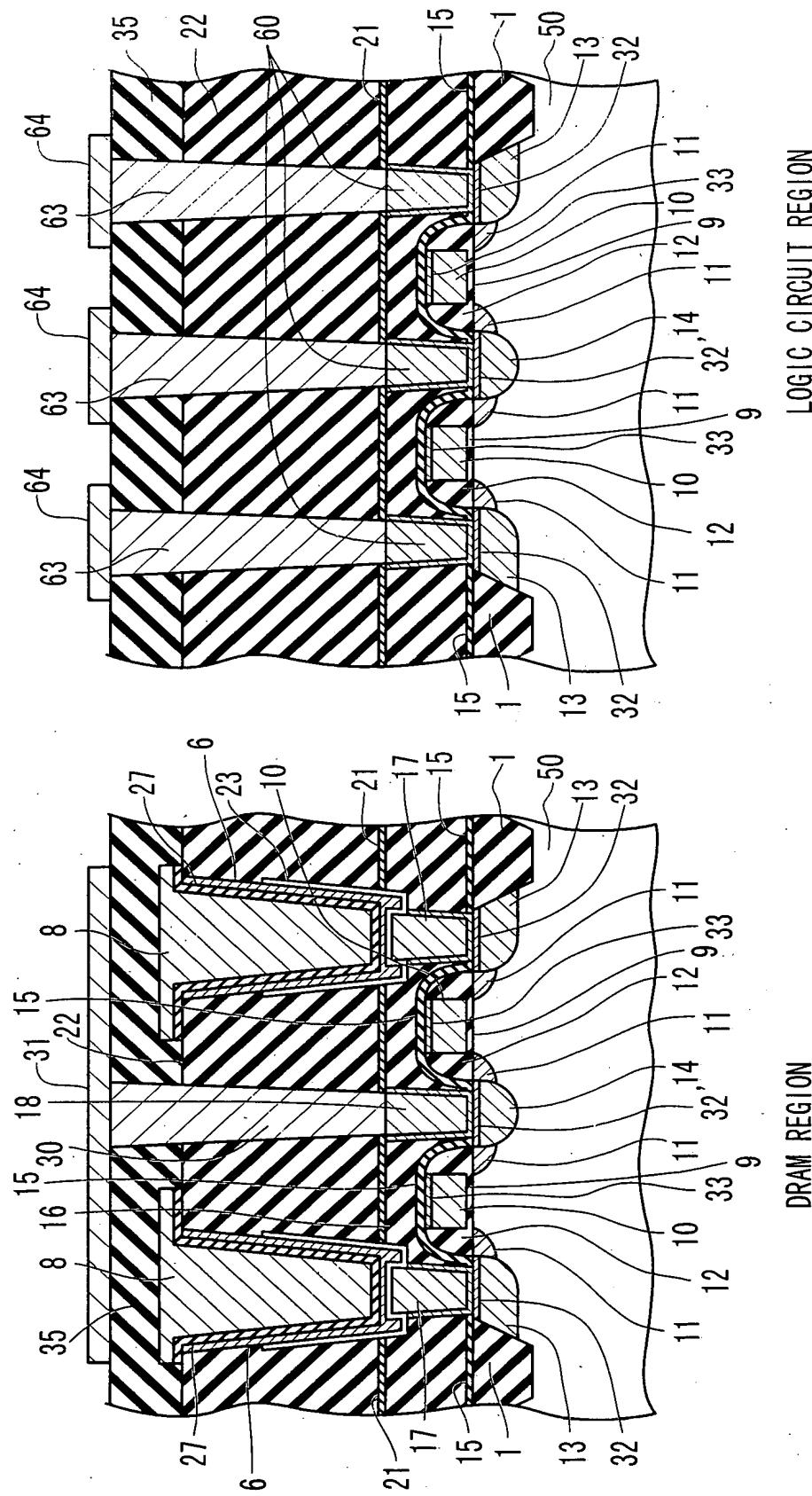


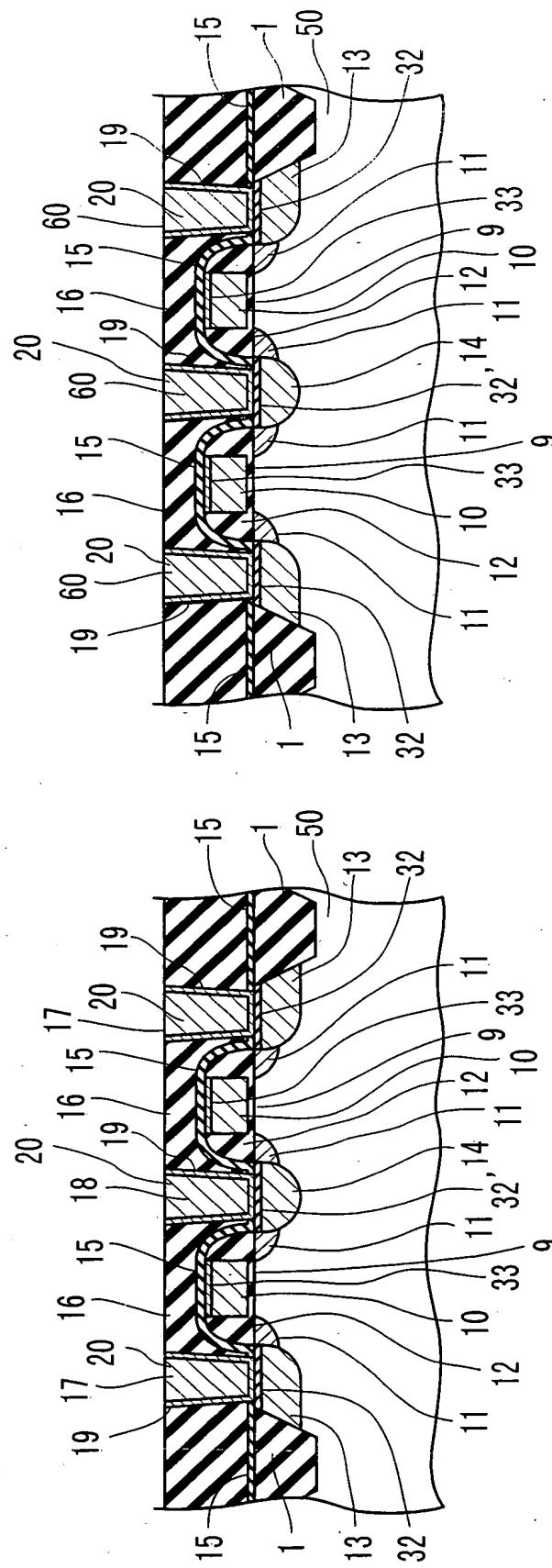
Fig. 16





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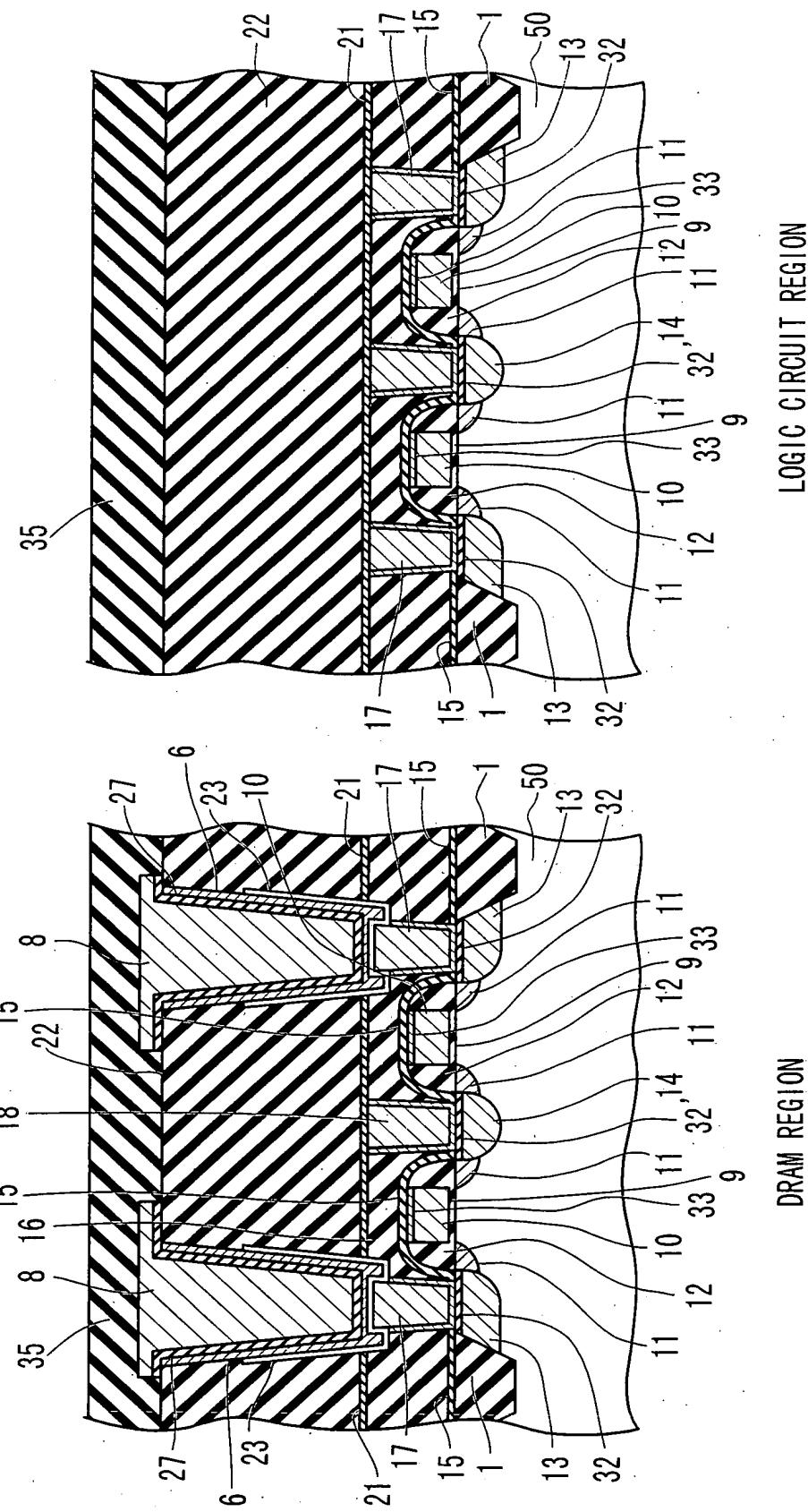


LOGIC CIRCUIT REGION

## DRAM REGION

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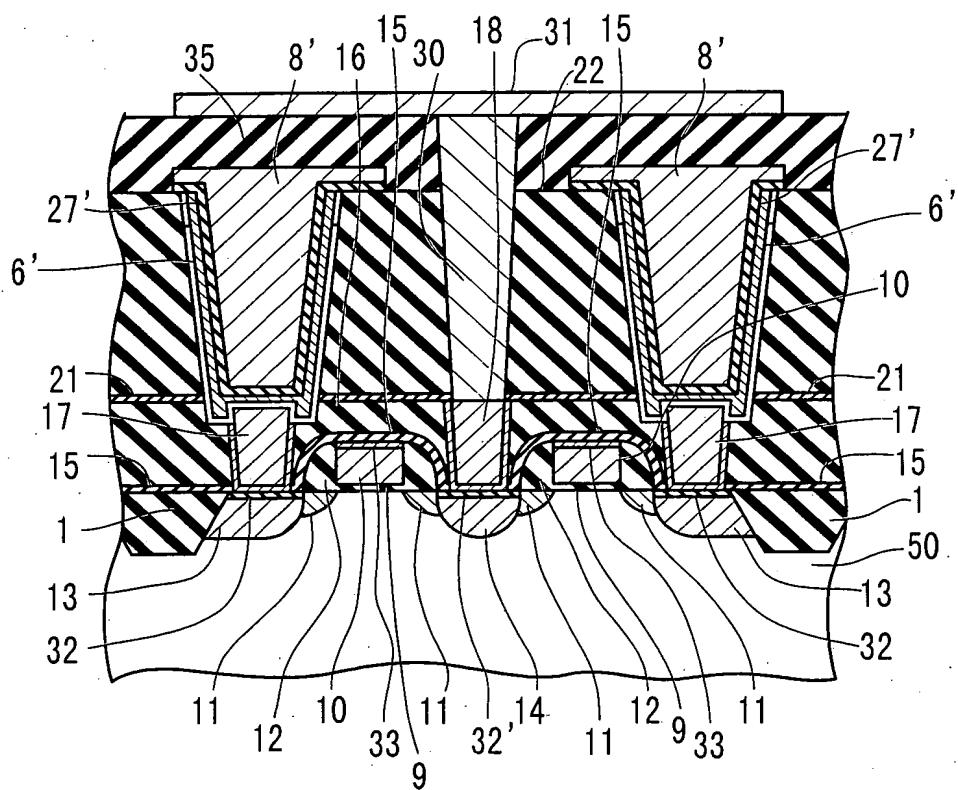
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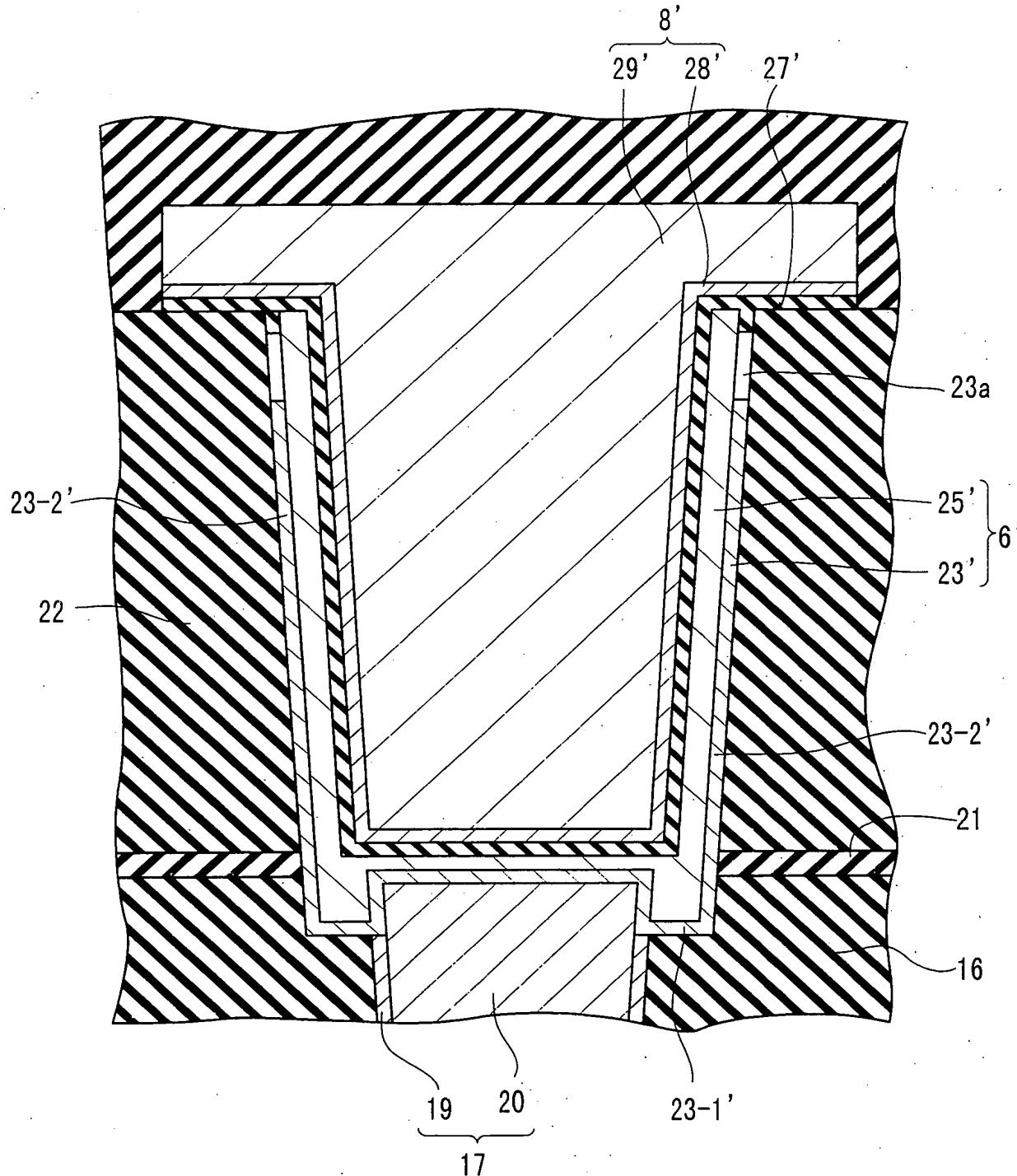
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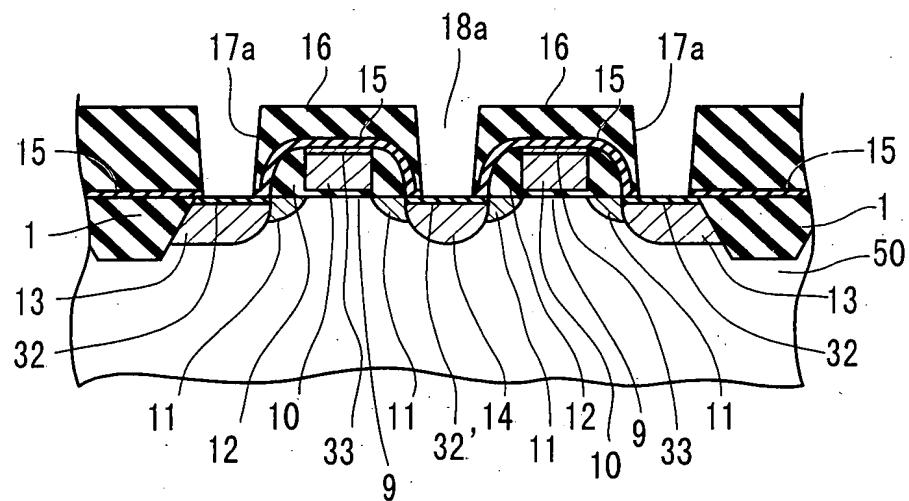
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Fig. 20



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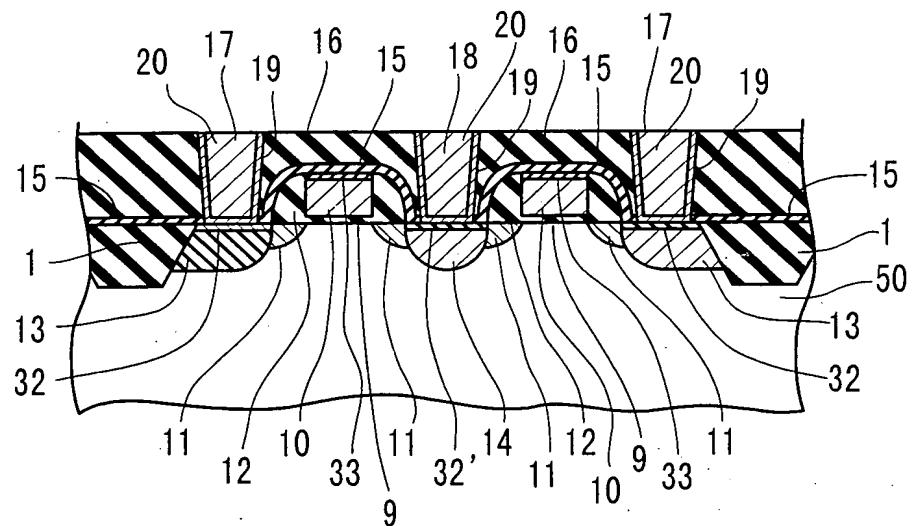
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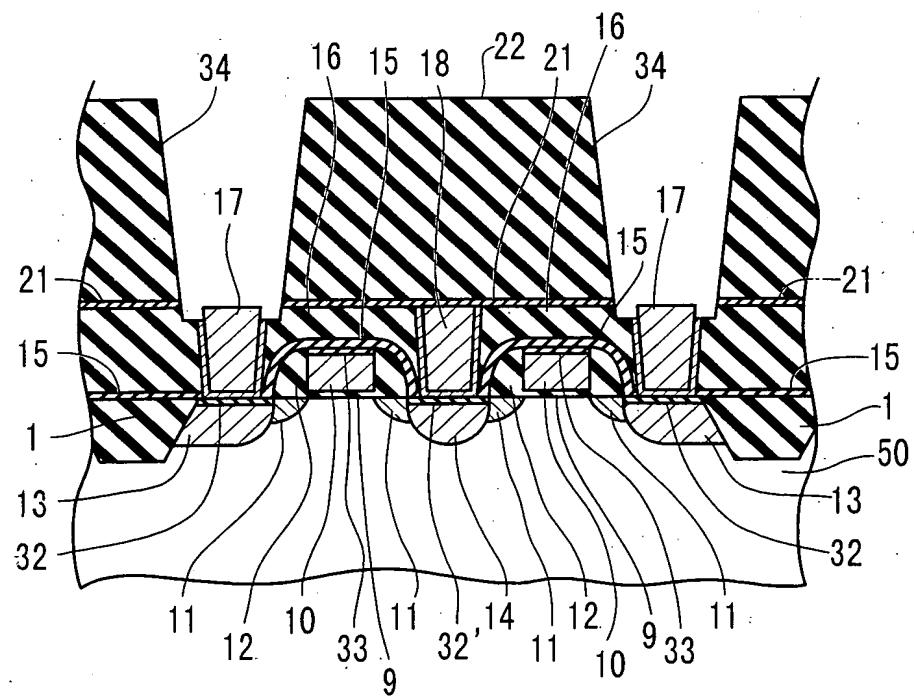
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Fig. 24

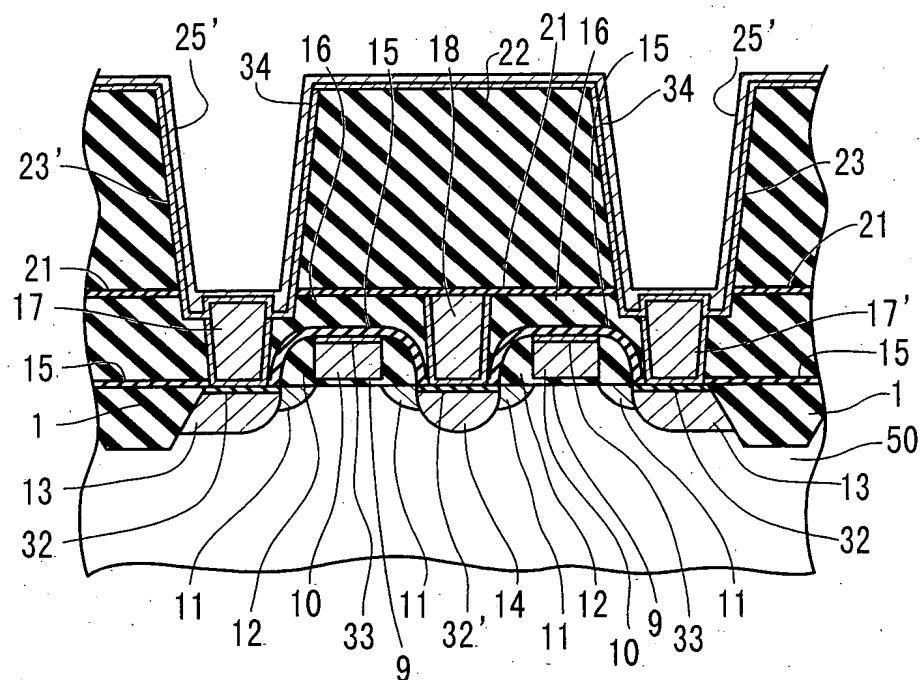


Fig. 25

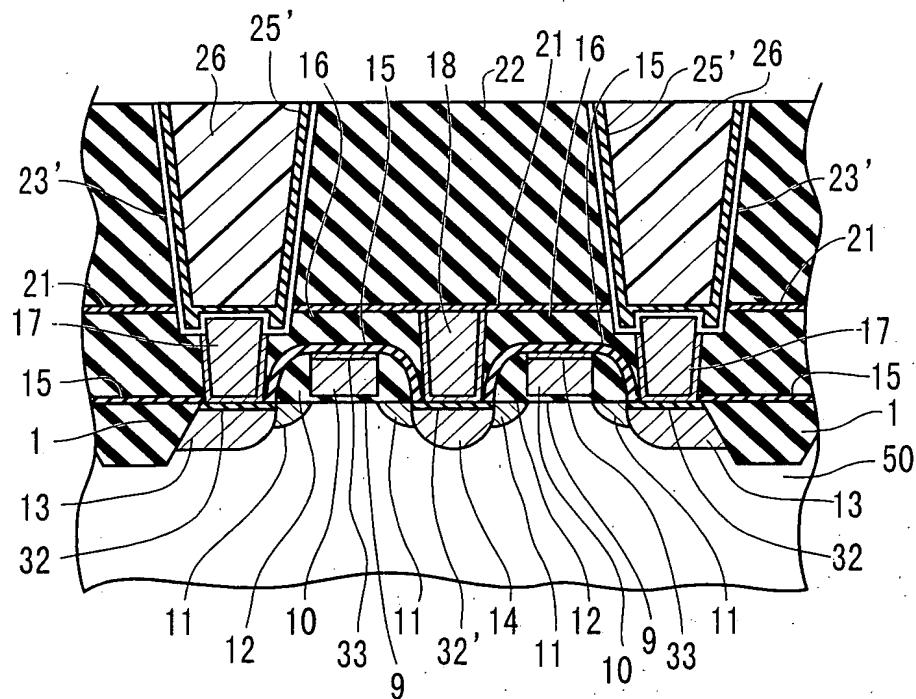
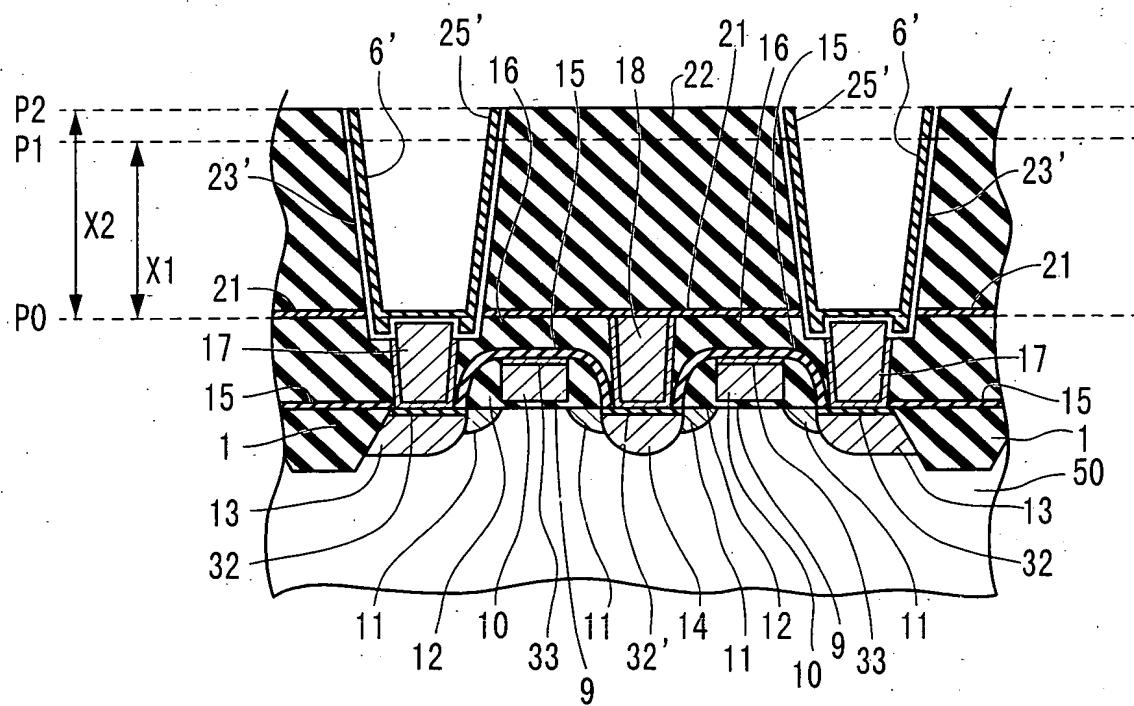


Fig. 26



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Fig. 27

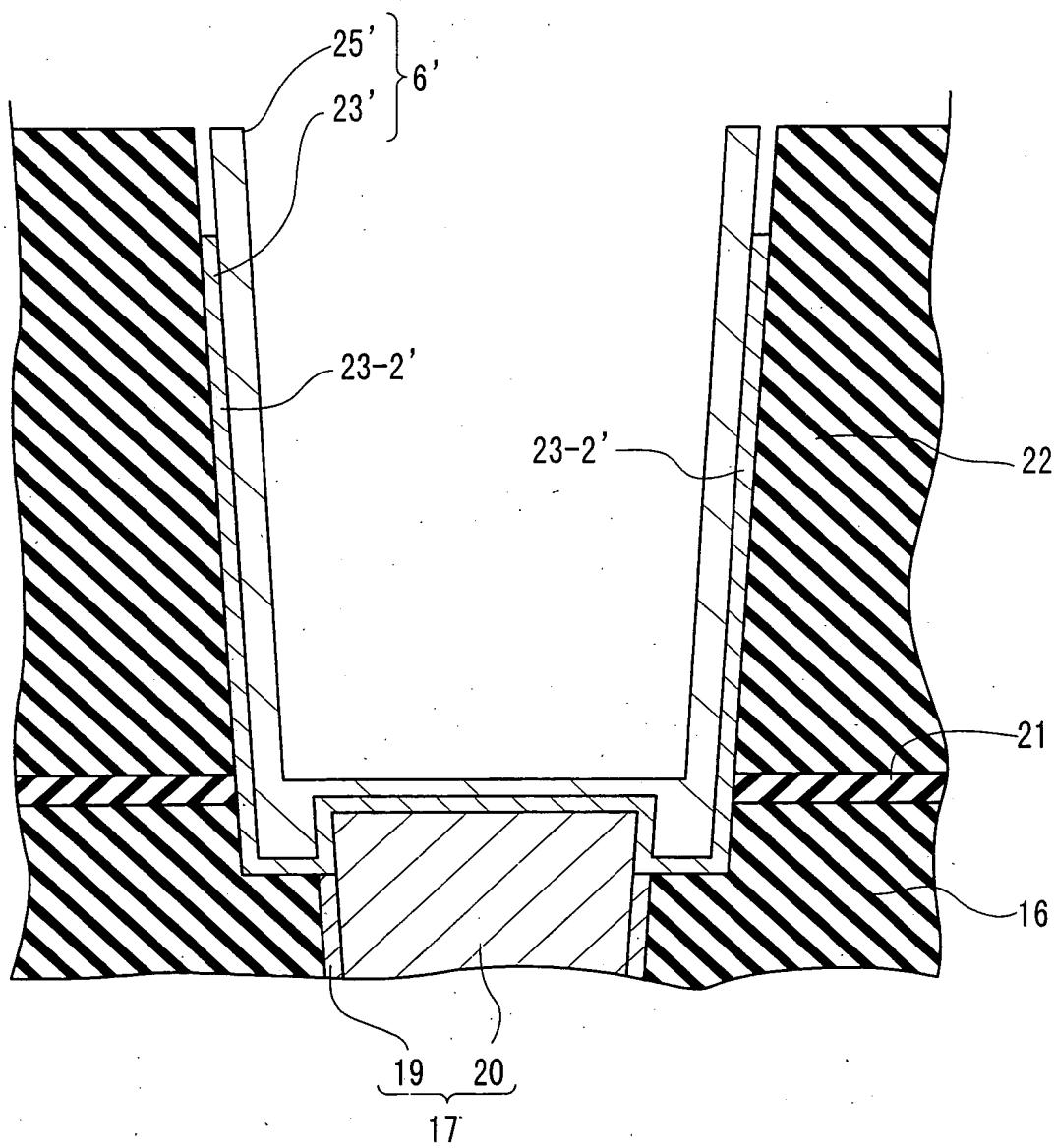
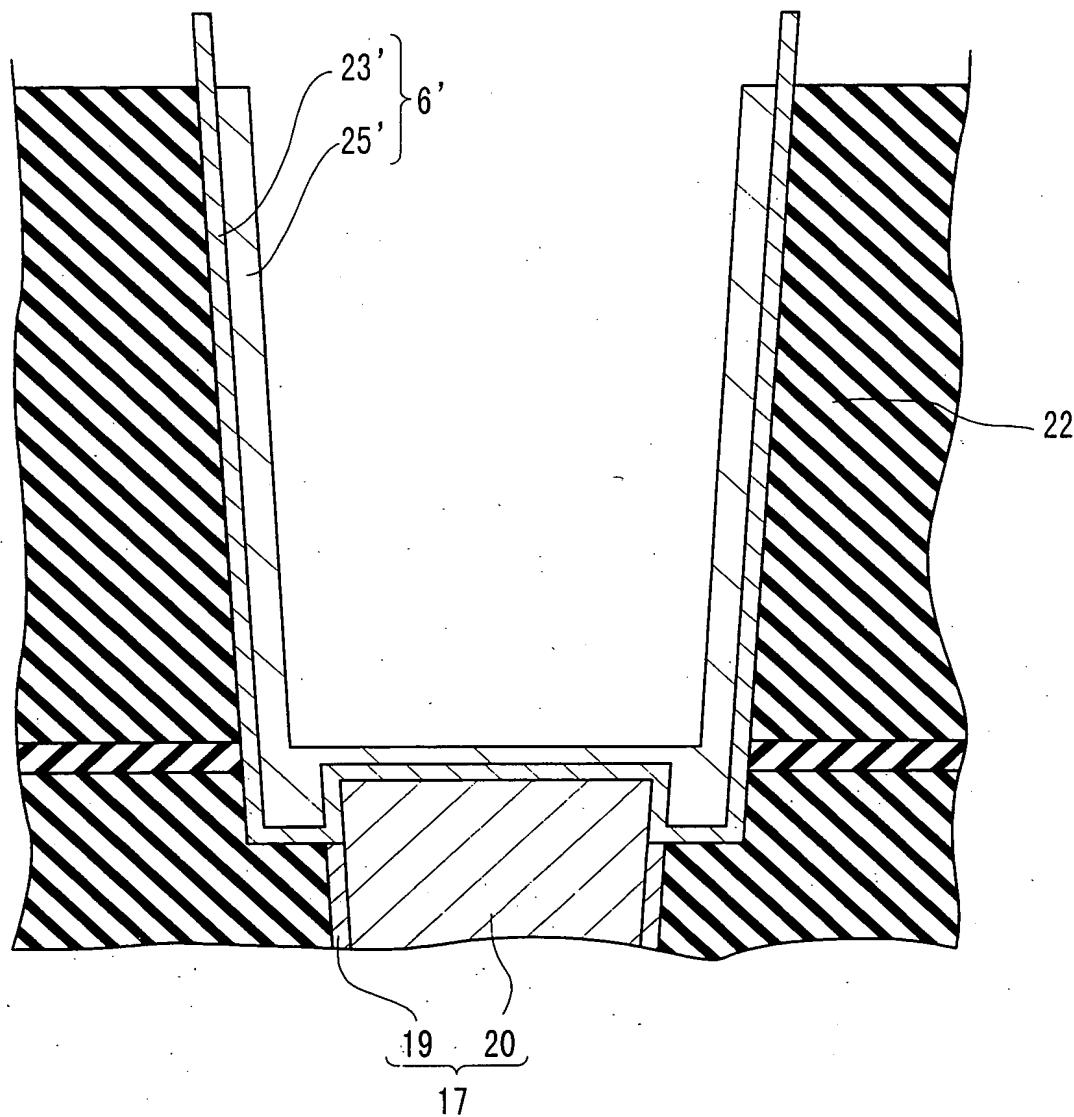


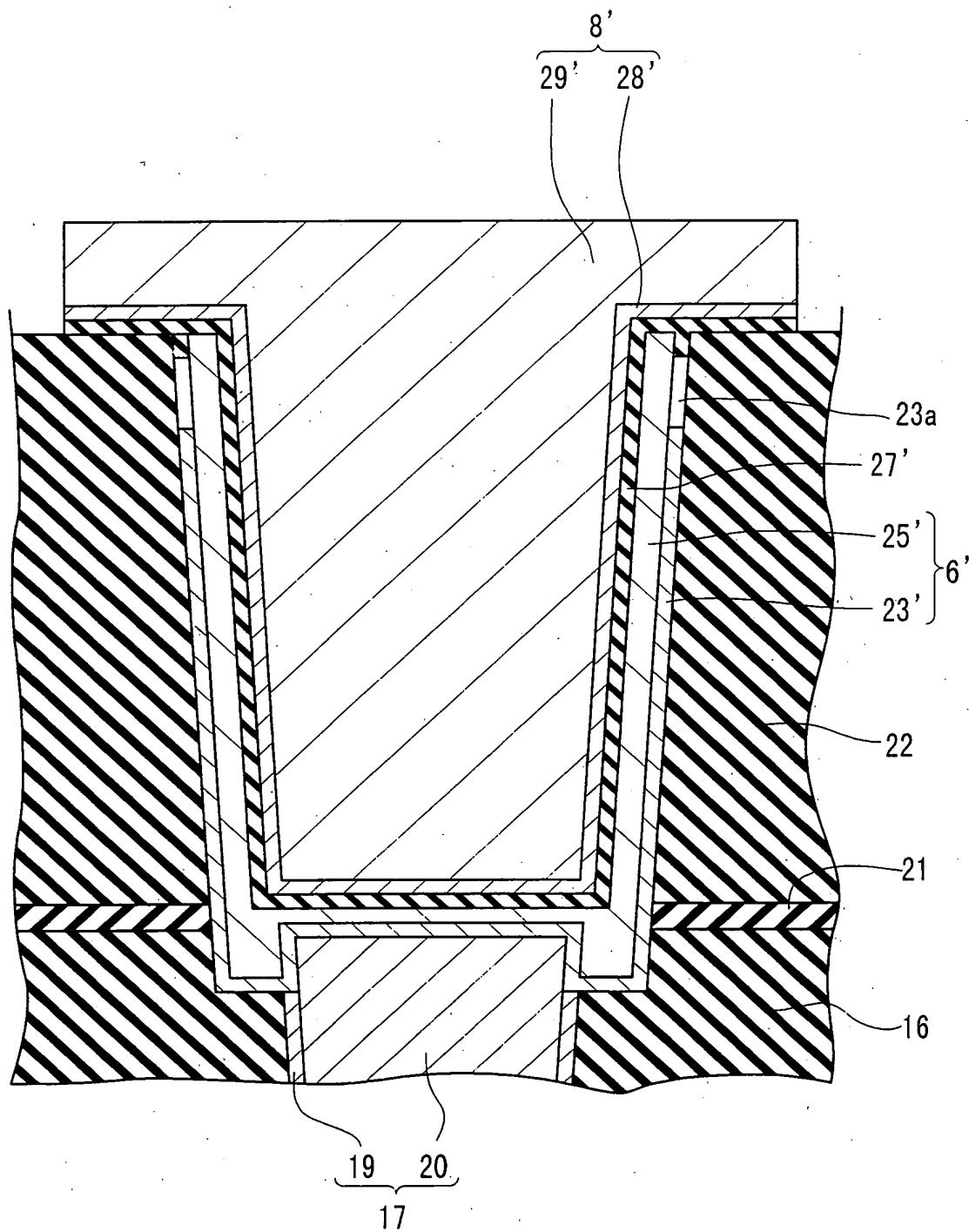
Fig. 28



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Fig. 29



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